CLAIMS

1. A semiconductor structure comprising:

a first semiconductor region characterized by a dopant concentration greater than $1x10^{19}/cm^3$;

a second semiconductor region overlying the first semiconductor region, said second semiconductor region comprising silicon and characterized by a dopant concentration less than $1x10^{19}/cm^3$ and a thickness t1; and

a layer comprising titanium directly overlying the second semiconductor region, said layer characterized by a line width no greater than 0.3μm and a thickness t2, wherein t1 > 1.2t2;

t1/t2 being sufficiently small that, when the layer is reacted with the second semiconductor region to form titanium disilicide, the titanium disilicide is in ohmic contact with the first semiconductor region;

t1/t2 being sufficiently large that, when the layer is reacted with the second semiconductor region to form titanium disilicide, the titanium disilicide anneals to a phase with a sheet resistance less than 3 ohms/square.

2. The invention of Claim 1 wherein $t1 \geq 2.2t2$.

3. The invention of Claim 1 wherein $t1 = 2.3t2, \pm 0.1t2$.

4. The invention of Claim 1 wherein t1 is about 600Å and t2 is about 250Å.

5. The invention of Claim 1 wherein the dopant concentration of the first semiconductor region is greater than $1x10^{20}/cm^3$.

6. The invention of Claim 1 or 5 wherein the first semiconductor region is doped primarily with boron.

7. A semiconductor structure comprising:

a first semiconductor region characterized by a boron dopant concentration greater than $1x10^{20}/cm^3$; and

a set of titanium silicide conductors directly overlying the first semiconductor region and in ohmic contact therewith, each said conductor characterized by a width no greater than 0.3μm, and at least 90% of said conductors characterized by a sheet resistance less than 3 ohms/square.

8. The invention of Claim 1 or 7 wherein the semiconductor structure comprises a 3-D memory array.

9. A method for forming a semiconductor structure, said method comprising:

(a) forming a first semiconductor region characterized by a dopant concentration greater than $1x10^{19}/cm^3$;

(b) forming a second semiconductor region overlying the first semiconductor region, said second semiconductor region comprising silicon and characterized by a dopant concentration less than $1x10^{19}/cm^3$ and a thickness t1;

(c) forming a layer comprising titanium directly overlying the second semiconductor region, said layer characterized by a line width no greater than 0.3μm and a thickness t2, wherein t1 > 1.2t2.

10. The method of Claim 9 further comprising:

(d) annealing the second semiconductor region and the layer at a temperature of at least 550°C after (c) , thereby forming TiS_{ix} from the titanium of the layer and the silicon of the second semiconductor region.

11. The method of Claim 10 further comprising:

(e) re-annealing the second conductor region and the layer after (d) at a temperature of at least 750°C, thereby converting the TiS_{ix} to C54 phase in ohmic contact with the first semiconductor region.

12. The method of Claim 9 wherein the first semiconductor region is formed in (a) with a dopant concentration greater than $1x10^{20}/cm^3$.

13. The method of Claim 9 or 12 wherein the first semiconductor region formed in (a) is doped primarily with boron.

14. A method for forming a semiconductor structure, said method comprising:

(a) forming a heavily doped first semiconductor region;

(b) forming a second semiconductor region comprising silicon and overlying the first semiconductor region, said second semiconductor region less heavily doped than said first semiconductor region and characterized by a thickness t1;

(c) forming a layer comprising titanium directly overlying the second semiconductor region, said layer characterized by a line width no greater than 0.3μm and a thickness t2, wherein t1 > 1.2t2; and

(d) annealing the second conductor region and the layer after (c) at a temperature of at least 750°C, thereby forming a low-resistivity, C54-phase TiS_2 film in ohmic contact with the first semiconductor region.

15. The method of Claim 9 or 14 wherein the semiconductor structure comprises a 3-D memory array.

16. The method of Claim 9 or 14 wherein $t1 \geq 2.2t2$.

17. The method of Claim 9 or 14 wherein $t1 = 2.3t2 \pm 0.1\ t2$.